REMARKS

An Office Action was mailed on October 18, 2004. Claims 1 – 8 are pending in the present application. In the present Response, Applicant cancels claim 1 without prejudice or disclaimer, amends claim 5 to include the limitations of canceled claim 1, amends claims 2 – 4 to depend from amended claim 5, and amends claim 8 to include the limitations of former claim 5. No new matter is added.

OBJECTED CLAIMS

Applicant thanks the Examiner for indicating that claims 6 and 7 are objected to as depending on rejected based claim 1, but that each would be allowable if rewritten to include all of the limitations of base claim 1 and any intervening claims. Claim 6 depends from claim 5, and claim 7 depends from claim 6.

Applicant amends claim 5 to include the limitations of canceled claim 1, and for the reasons stated below, respectfully submits that amended claim 5 is allowable. As amended claim 5 is allowable, Applicant further submits that objected claims 6 and 7 are allowable for at least this reason. Accordingly, Applicant respectfully requests that the objection be withdrawn.

REJECTION UNDER 35 U.S.C. §§ 102, 103

Claims 1 – 5 and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,841,522 to Yamazaki. Claims 1 – 5 and 8 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,021,135 to Ishihara et al. in view of Yamazaki. Applicant cancels claim 1 without prejudice or disclaimer, amends claim 5 to include the limitations of canceled claim 1, amends claims 2 – 4 to depend

from amended claim 5, amends claim 8 to include the limitations of former claim 5, and respectfully traverses these rejections.

In amended independent claim 5, for example, Applicant discloses:

> **5.**A cross-connection switch comprising:
>
> first memory means for storing data indicating switching information of a time slot at an address to which time slot information is assigned;
>
> second memory means for storing data of each time slot of an input frame in time slot units, inputting data stored in said first memory means, and outputting the data stored at the address specified by the data as time slot data of an output frame;
>
> counter means for counting a number of input time slots of an input frame in synchronization with the input frame, and outputting the count value as a read address and a write address respectively to said first memory means and said second memory means; and
>
> The switch according to claim 1, further comprising
>
> selector means for switching data of a time slot directly input from an input line with data of a time slot read from said second memory means and outputting a switching result, wherein
>
> said selector means is controlled to output time slot information not to be switched as time slot data of an output frame <u>without performing a process on the information</u> by inputting information read from said first memory means as a selector signal to said selector means, and to output time slot data read from said second memory means as time slot data of an output frame to be switched.
>
> (Emphasis added)

Yamazaki discloses a time division channel switching circuit (see, e.g., abstract of Yamazaki). As illustrated in FIG. 1 of Yamazaki, input signals from a plurality of channels are multiplexed by multiplexing circuit 34, converted from serial to parallel format by S/P converter 36, and duplicately stored in channel memories 31-1-1 through 31-1-n in time switch 31-1. T-control memory 31-1-2 read the channel memories by providing a corresponding address to the channel memories, and a corresponding signal

is read from the channel memories and output to output highways via selector 32-1, P/S converter 37 and distribution circuit 35. By duplicately storing the signals, switching can be effectively accomplished without the use of a high-speed memory.

In order to enable switching among a plurality of channels, the device of Yamazaki performs multiplexing and serial to parallel conversion prior to writing data to the memories, and preforms parallel to serial conversion and demultiplexing after reading data from the memories. In sharp contrast, in Applicant's claimed switch of amended claim 5, data is read directly into the second memory and read out of the second memory without operations directed to multiplexing/demultiplexing and serial to parallel/parallel to serial conversion. This is accomplished by virtue of Applicant's claimed selector means, which switches data of a time slot directly input from an input line with data of a time slot read from said second memory means in order to output a switching result.

In addition, Applicant's claimed switch differs from the device of Yamazaki in another important aspect. In the device of Yamazaki, each data signal is read into the memories, and then read out of the memories, regardless of whether any time slot switching is required. In sharp contrast, in Applicant's claimed switch, the claimed selector means operates such that data signals requiring no time slot switching are read from the input line directly into the selector without being read from the second memory. This approach reduces signal delays over the fully switched approach taught by Yamazaki.

Accordingly, Applicant respectfully submits that the device of Yamazaki fails to anticipate Applicant's switch as claimed in amended independent claim 5, and that amended independent claim 5 is therefore allowable. As amended independent 8 shares

the features discussed above in relation to amended claim 5, Applicant substantially reapplies the above arguments and submits that amended independent claim 8 is also allowable.

Ishihara discloses cell assembly and multiplexing/demultiplexing device (see, e.g., abstract of Ishihara. While the device of Ishihara includes a selector (see, e.g., column 8, lines 25 – 50 of Ishihara describing selector 30 of FIG. 6), Applicant respectfully submits that Ishihara's selector fails to meet the limitations of Applicant's claimed selector means. Specifically, Ishihara fails to disclose that selector 30 operates such that data signals requiring no time slot switching are read from an input line directly into the selector without being read from the second memory, while data signals requiring time slot switching are read from the memory. Rather, selector 30 is used to select among components required for the assembly of an ATM frame. Accordingly, Applicant submits that the addition of Ishihara to Yamazaki fails to teach or suggest Applicant's claimed switch including Applicant's claimed selector means, that claims 5 and 8 are therefore not obvious in view of Ishahara and Yamazaki, and are therefore allowable.

Dependent claims 2 – 4 depend from allowable claim 5. For at least this reason, Applicant respectfully submits that dependent claims 2 – 4 are allowable.

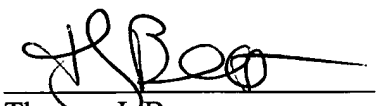
CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that 2 - 8, which include independent claims 2 and 8, and the claims that depend therefrom, stand in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in

condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



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Docket No.: 100794-11328 (FUJO 16.572)